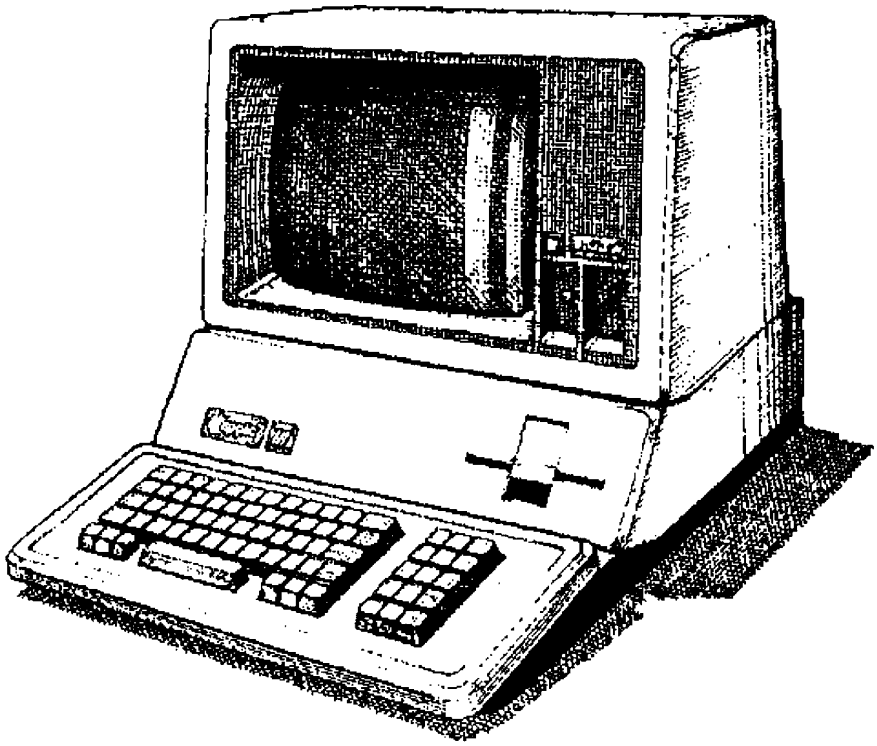
Apple /// Computer Information

Apple /// Service Reference Manual



Section I of II • Theory of Operation

Chapter 4 • The ACIA

Written by Apple Computer • 1982

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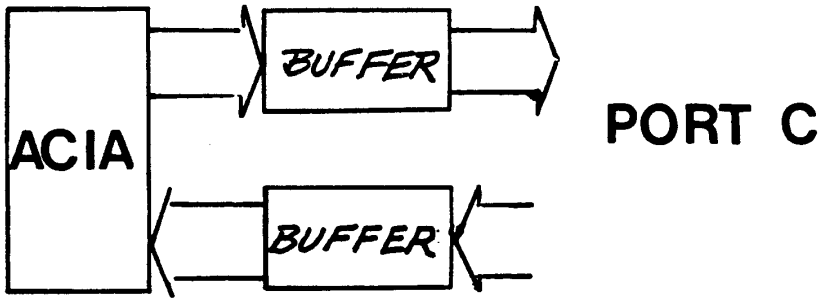
THE 6551 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER

As you know, the Apple /// can be used to communicate to all devices that use the RS-232-C standard communications format. This means the Apple /// can communicate with letter-quality printers, modems, high speed data collection devices, and other computers. The Apple /// has a built in Asynchronous Communications Interface Adapter (ACIA). It is located at addresses C0F0 through C0F3. This device is solely for use as a serial port input/output controller. This RS-232-C protocol, specified by the Electrical Industries Association (EIA), is provided at port C connector through two buffer devices as shown below.



The 6551 contains seven registers and five control circuits dealing with the control, timing, and interrupt logic of transmitting amd receiving data through the serial EIA port. A block diagram of the 6551 ACIA is shown in Figure 1.

Before using the 6551, the system (or programmer) must initialize it for the I/O mode. Once initialized it will be set to transmit and/or receive data within the parameters set in the control bytes.

The Apple /// I/O addresses for data and control are presented in the following discussions. The function of the data byte (depending on location) will also be shown. The characters in parentheses next to each register represent the function of the associated pin of the ACIA (i.e. R=Read,W=Write).

RECEIVE DATA REGISTER (RxD)

The Receive Data Register is accessed with I/O location C0F0 (r). The contents of the Receive Data Register will be the data bits of the completely received serial input character. This register is used as temporary data storage for the 6551 receive circuit. The first data bit received will be the LSB of the data byte (Bit 0).

C0F0 (R) RECEIVE DATA REGISTER

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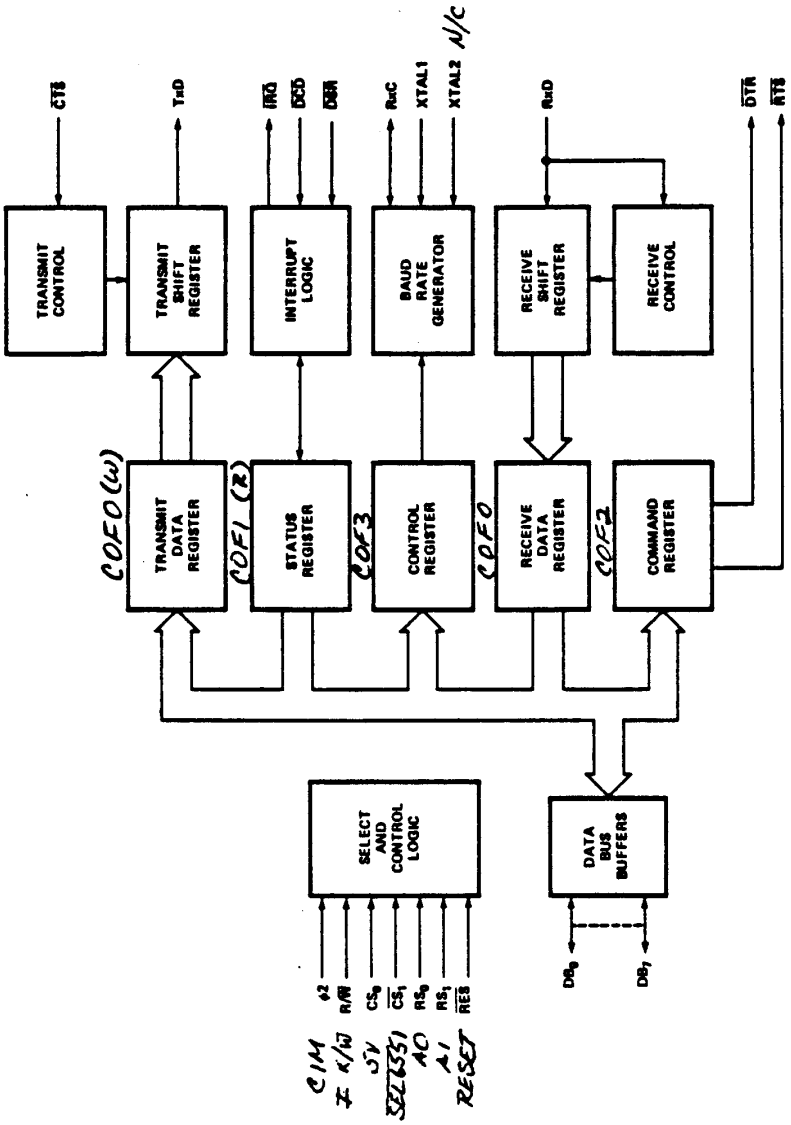

FIG 1

THE ACIA BLOCK DIAGRAM

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TRANSMIT DATA REGISTER (TxD)

To load a byte to be transmitted out the serial EIA port, I/O location C0F0 (w) must be accessed. The LSB will be the first data bit transmitted.

C0F0 (w) TRANSMIT DATA REGISTER (w)

STATUS REGISTER

The 6551 continually monitors the condition of the registers and the quality of the incoming data. When I/O location C0F1 (R) is accessed the contents of the Status Register is placed on the data bus. The meanings of the eight bits of the status byte are detailed following the illustration.

C0F1 (R) STATUS REGISTER

IRQ--Bit 7 indicates that the 6551 generated an IRQ to the system for one of the folllowing conditions:

1. Change of status of the DCD line.
2.. Change of status of the DSR line.
3. The Transmit Register has emptied.
4. The Receive Register has filled with a new incoming character.

(Note: the third and fourth conditions are program controlled as to whether or not they inititate an IRQ).

DSR---Bit 6 indicated the status of the DSR line from the interface. 0=DSR is low and ready. 1=DSR is high and not ready.

DCD---Bit 5 shows the condition of the Data Carrier Detect line from the interface. 0=DCD is low and the carrier is detected. 1= DCD is high and not ready.

TDRO--Bit 4 informs the host that the Transmit Data Register has transferred its contents to the outputs shift register and now ready to accept another character (byte). 0=not empty, 1=empty.

RDRF1-Bit 3 indicates that the Received Data Register has been filled with a character from the line. 0=not full, 1=full.

OVERR-Bit 2 shows that there has been an overrun error, that is, a new character has been transferred to the Received Data Register before the previous received character was taken by the program and the RDRF1 flag reset. This error will not generate an IRQ but should be checked by the program so that tht lost data can be recovered. 0=no overrun, 1= overrun has occurred.

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FRMERR-Bit 1 informs the program that the incoming data did not conform to the parameters set in the Control Register. That means usually that when the 6551 checked for the position and number of stop bits if found a descrepency. This error most often happens when the remote device is transmitting at a different baud rate. 0=no framing error, 1=framing error detected. This error does not generate an IRQ.

PARERR--Bit 0 indicates that there has been a parity error in the incoming data. This error does not cause an IRQ to be generated. 0=no parity error,1=parity error detected.

PROGRAMMED RESET

By accessing COF1 (w) the Status Register will be reset to all 0's. The data byte on the bus at that cycle does not have to be any particular structure.

COF1 (w) PROGRAMMED RESET (w)

COMMAND REGISTER

To access the Command Register to initialize or modify the Command byte a COF2 (w) must be executed with the data byte configured for the desired effect. To inspect the contents (or current command structure) a COF2 (R) will cause the 6551 to place the contents of the Command Register on the data bus. The meaning of each bit is explained below.

COF2 (r/w) COMMAND REGISTER (r/w)

Parity ck ctrls--Bits 7 through 5 command the 6551 in regard to parity checking. Bit 5 is parity enable. Bit 7 determines whether the parity bit position will have odd/even or fixed one/zero function. Bit 6, depending on the condition of Bit 7 selects either odd or even parity, or fixed mark (one) or fixed zero (space). Table -- below clearly shows the conditions of these bits.

ECHO--Bit 4 determines whether the 6551 will echo (transmit a duplicate image of what is received) the received data to the remote device. 0=no echo, 1=echo data.

TRANS CTRLS--Bits 3 and 2 control the 6551 in three (3) functions. They are Transmit Interrupt, the state of the RTS line, and the Transmit BRK (break, a continuous space on the line for approximately 200 milliseconds). Table -- shows which state controls which function.

INT--Bit 1 command the 6551 to either enable or disable interrupt on Received Data Register full (bit 3 of the status byte). 0=IRQ on RDRF1, 1=no interrupt.

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DTR--Bit 0 enable the 6551 to transmit and receive or not. It also changes the state of the DTR output to match the condition of the 6551. 0=disable xmit/rcv (DTR high), 1=enable Xmit/Rcv (DTR low).

CONTROL REGISTER

The final I/O location on the 6551 is the Control Register. By writing to CPF3 (w) with a properly structured date byte four functions are controlled. They are Number of Stop bits appended to outgoing data byte (and checked for on the incoming date byte), the source of the receiver clock, and the baud rate selection. By reading location COF3 (x) the current control configuration can be seen on the data bus.

COF3 (R/W) CONTROL REGISTER (R/W)

STOPB--Bit 7 controls the number of stop bits that will be added to the transmitted data word. 0=1stop bit, and depending on the word length selection 1=2 stop bits or 1 bit if word length is 8 and parity is selected, or 1/2 bits if word length is 5 and no parity is selected.

WORD LEN--Bits 6 and 5 determine the number of data bits that will be transmitted or received in the data word. The values (6,5) are as follows: 0,1=7 bits; 1,0=6 bits; 1,1=5 bits.

'XCLK--Bit 4 indicates the source of the receiver clock. 0=external clock source, 1=baud rate generator (internal). When the internal selection is made the RxC pin becomes an output.

BAUD RATE--Bits 3 through 0 select the baud rate at which the 6551 will operate. Table -- details the various selections available based on a standard 1.8432 MHZ clock input. It should be noted that 0,0,0,0 selects the external clock as the baud rate source but the clock rate is actually dividied by 16 so the external clock should be 16x the desired baud rate.

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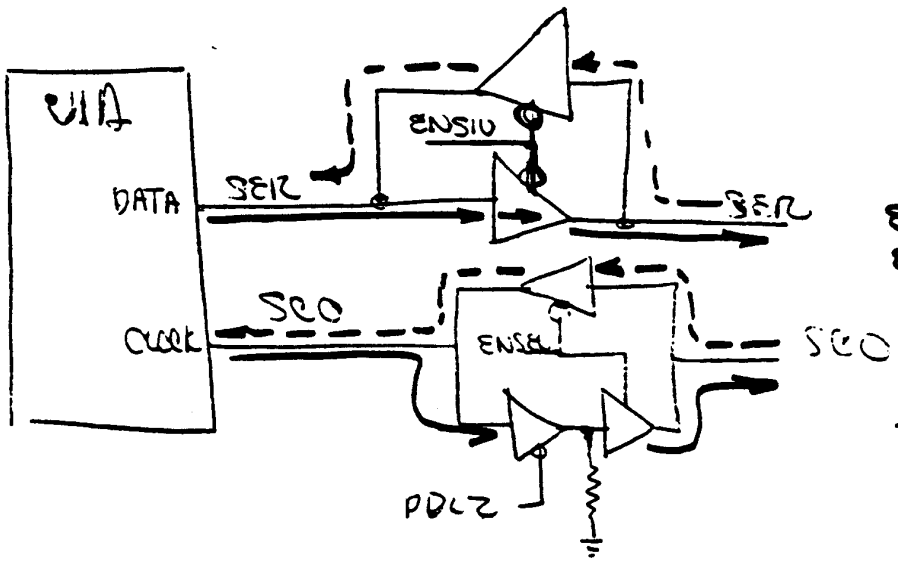
SIMPLE SERIAL PORT

Incorporated into the A /// logic design is a provision for a simple serial port. Its main purpose is to support a Silentype printer. However, it is not a dedicated port since it shares the same connector with one of the joysticks. The user has the option of having the Silentype or a second joystick. For most applications, one joystick is more than enough since the A /// is not really intended for a "games" player. The joystick would be used more for applications like cursor control.

The serial port is actually derived from a feature of the VIA. Two of the port control lines (PB1, PB2) can be configured to be a shift register, hence a simple serial port (see the section on VIA's and read the spec sheet in the appendices). In the system certain other software controlled switches must be set to enable the port. These switches are found in another addressable latch (U177). They control the direction of data and clock to and from the board. The VIA is programmed internally to determine its function.

The signal ENSIO when high enables data from the VIA to the port, when low it enables data from the port to the VIA. The signal ENSEL determines the direction of the clock, high enables clock from the VIA to the port (if and only if PDL2 is low), low enables the port to supply the clock to the VIA. ENSEL when high also enables the AXCO signal to the port, this can be used as a select or acknowlege to the remote device. The remote device may put status bits on the "switch" line which can be used to notify the processor of some requirement mutually agreed upon.

SIMPLE SERIAL PORT —



DATA
ENSIO=1 = OUT
ENSIO=0 = IN

CLOCK
ENSEL=1 = OUT
ENSEL=0 = IN

* IF PDL2 = 0
IF PDL2 = 1
THE OUTPUT
HELD LO.

NOTE: THE VIA MAY SEND DATA USING IT'S OWN CLOCK OR IT MAY BE SHIFTED WITH A REMOTE CLOCK.

ALSO IT MAY STROBE DATA IN WITH IT'S OWN CLOCK OR IT MAY BE STROBED IN WITH A REMOTE CLOCK

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PINOUT OF THE RS-232-C SERIAL INTERFACE (PORT C)

PIN	NAME	DESCRIPTION
1	SGND	Shield GrouND.
2	TXD	Transmitted Data; serial data output from the Apple.
3	RCD	ReCieved Data; serial input to the Apple.
4	RTS	Request To Send output; this indicates that the Apple is ready to transmit data. This line is active whenever the Serial Card emulation is used.
5	CTS	Clear To Send input; this acknowledges that the Apple may begin transmission. This line is ignored by the Serial Card emulation.
6	DSR	Data Set Ready input; this acknowledges that the remote device is operational. The Serial Card emulation checks this line and will not send characters if this line is held inactive. This can be used to prevent the Apple from overflowing a printer input buffer.
7	GND	Signal GrouND.
8	DCD	Data Carrier Detect; this acknowledges that the remote device is ready to transmit data. The Serial Card emulation checks this line and will not send characters if this line is held inactive. This line can be used to prevent the Apple from overflowing a printer input buffer.
9-19		No connect.
20	DTR	Data Terminal Ready output; this indicates that the Apple is on and operational. This line will be active anytime the Serial Card emulation is used.

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THE ACIA

The Apple /// has a built-in 6551 ACIA (Asynchronous Communication Interface Adapter). It is located at addresses $C0F0 thru $C0F3 (decimal -16144 to -16141). The ACIA has five registers: transmit data, receive data, status, command, and control.

The transmit register ($C0F0) is used to send data out the Apple /// to an external device, such as a modem or a printer. A byte is transmitted by setting the control and command registers appropriately and then polling the status register. When bit 4 of this register is one the ACIA is ready to shift the next byte out. Often bits 5 and 6 are tested for zero to assure the Data Carrier Detect and Data Set Ready are valid as some printers use these lines as handshake signals.

Care must be taken when writing to the transmit data register as it is at the same address as the receive data register. The 6502 will do false reads when certain address modes are used, thus discarding whatever was in the receive data register.

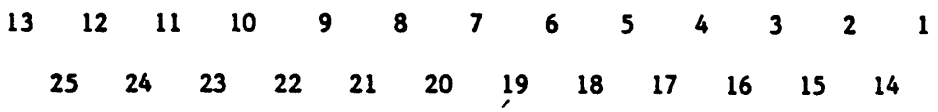
The receive data register ($C0F0) contains the last byte received from an external source, such as a modem. Bit 3 of the status register is one whenever this register is full.

The status register ($C0F1) indicates the states of Data Set Ready, Data Carrier Detect, whether the transmit and receive registers are full, and whether a framing, overrun or parity error has occured on input.

The command register ($C0F2) sets the parity, echo mode, transmit and receive enables, and BRK transmission.

The control register ($C0F3) sets the number of stop bits, data word length, receiver clock source, and baud rate.

PHYSICAL PINOUT OF THE RS-232-C SERIAL INTERFACE



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RS232 CONNECTOR USAGE (PORT C)

The Apple /// is classified as Data Terminal Equipment (DTE) under the EIA RS-232-C interface specification. It can be directly connected to a piece of Data Communications Equipment (DCE), such as a modem. To connect the Apple to another piece of Data Terminal Equipment (such as a printer), you must use a modem eliminator.

All output levels are minimum +6 volts when logic 0 and maximum -6 volts when logic 1, measured into a 3K ohm load.

All inputs have a turn-on positive going threshold of +1.25 volts and a turn-off negative going theshold of +.8 volts, typical. All inputs sink a 10 mA current, maximum.

CONTROL REGISTER

The Control Register is used to select the desired mode for the SY6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

C0F3

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity.

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

BAUD RATE GENERATOR

3	2	1	0	
0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

*This allows for 9-bit transmission (8 data bits plus parity).

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

Figure 6. Control Register Format

COMMAND REGISTER

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

C0F2

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	Parity Disabled - No Parity Bit Generated - No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

DATA TERMINAL READY

0 = Disable Receiver/Transmitter (DTR high)
1 = Enable Receiver/Transmitter (DTR low)

RECEIVER INTERRUPT ENABLE

0 = IRQ Interrupt Enabled from Bit 0 of Status Register
1 = IRQ Interrupt Disabled

TRANSMITTER CONTROLS

BIT 3	BIT 2	TRANSMIT INTERRUPT	RTS LEVEL	OTHER
0	0	Disabled	High	–
0	1	Enabled	Low	–
1	0	Disabled	Low	–
1	1	Disabled	Low	Transmit BRK

NORMAL/ECHO MODE FOR RECEIVER

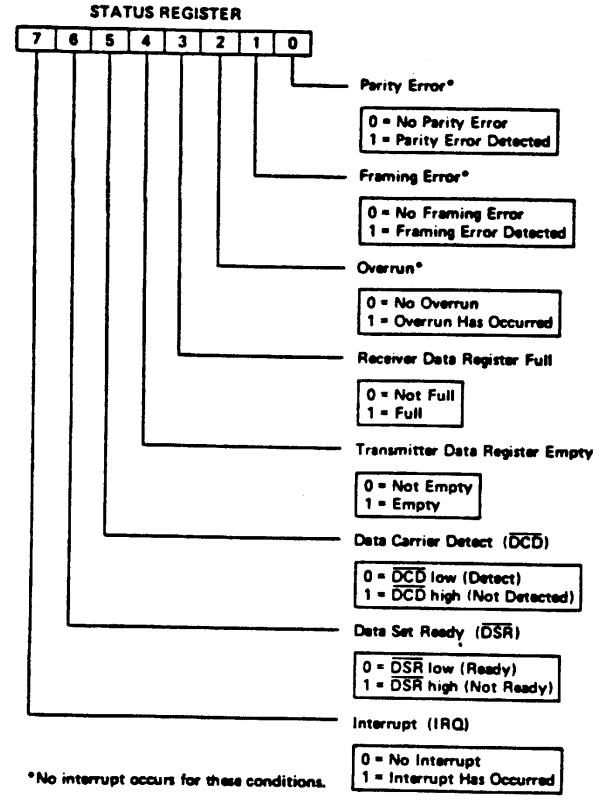
0 = Normal
1 = Echo

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	1	0
PROGRAM RESET	–	–	–	0	0	0	1	0

Figure 7. Command Register Format

STATUS REGISTER C0F1

The Status Register is used to indicate to the processor the status of various SY6551 functions and is outlined in Figure 8.



	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

Figure 8. Status Register Format

PIN CONFIGURATION